AMENDMENTS to the CLAIMS

1. (Presently Amended): An integrated circuit device comprising:

a bond pad structure including:

a conductive pad;

a first doped region of a first conductivity type disposed in a semiconductor substrate of a second conductivity type, wherein the first doped region is underlying and surrounding the conductive pad;

a conductive region of the first conductivity type, underlying and surrounding the conductive pad, disposed in the first doped region;

a first tap region spaced apart from and surrounding a substantial portion of the first doped region, wherein the first tap region is electrically coupled to a first supply voltage;

an output driver transistor having a drain region and a source region, wherein the drain region is electrically coupled to the conductive pad; and

a second tap region surrounding the output driver transistor, wherein the second tap region is electrically and physically coupled to a second supply voltage and the source region.

2. (Presently Amended): The integrated circuit device of claim 1 wherein the conductive pad includes a metal ~~first and second supply voltages are ground~~.

3. (Presently Amended): The integrated circuit device of claim ~~1~~2 wherein the first tap region completely surrounds the first doped region, and wherein the first and second supply voltages are ground.

4. (Previously Presented): The integrated circuit device of claim 1 wherein the first tap region is a discontinuous region.

5. (Previously Presented): The integrated circuit device of claim 1 wherein a doping concentration of the first doped region is less than a doping concentration of the conductive region.

6. (Previously Presented): The integrated circuit device of claim 1 wherein the first tap

region is a second doped region and the second tap region is a third doped region.

7. (Previously Presented): The integrated circuit device of claim 6 wherein the second doped region is of an opposite conductivity type than the first doped region.

8. (Previously Presented): The integrated circuit device of claim 6 wherein the third doped region is a P type doped region and the output driver transistor is an NMOS type transistor.

9. (Previously Presented): The integrated circuit device of claim 1 further including a tap region portion that is spaced apart from and surrounding the first doped region, wherein the tap region portion is decoupled from the first supply voltage to provide a predetermined resistance between the first doped region and the first supply voltage.

10. (Previously Presented): The integrated circuit device of claim 1 wherein a portion of the second tap region is integrated into the source region.

11. (Previously Presented): The integrated circuit device of claim 10 wherein the first tap region is a discontinuous region.

12. (Presently Amended): A bond pad for an integrated circuit device, the bond pad comprising:

a conductive bonding layer;

a first doped region of a conductivity type formed in a semiconductor substrate of a second conductivity type, wherein the doped region is underlying and surrounding the conductive bonding layer;

a conductive region of the first conductivity type disposed in the first doped region, wherein the conductive region is underlying and surrounding the conductive bonding layer and wherein the conductive region includes a surface area at least substantially equal to a surface area of the conductive bonding layer; and

a conductive tap region spaced apart from and surrounding at least a portion of the first doped region, wherein a portion of the conductive tap region is electrically coupled to a supply voltage.

13. (Previously Presented): The bond pad of claim 12 wherein the supply voltage is a ground voltage and the conductive bonding layer includes a metal.

14. (Previously Presented): The bond pad of claim 12 wherein the doping concentration of the doped region is less than the doping concentration of the conductive region.

15. (Previously Presented): The bond pad of claim 12 wherein the conductive tap region is doped to be of an opposite conductivity type than the first doped region.

16. (Previously Presented): The bond pad of claim 12 further including a conductive tap region portion that is spaced apart from and surrounding the doped region, wherein the conductive tap region portion is decoupled from the supply voltage to provide a predetermined resistance between the doped region and the supply voltage.

17. (Previously Presented): The bond pad of claim 12 wherein the conductive tap region is a continuous region.

18. (Previously Presented): The bond pad of claim 17 wherein the conductive tap region completely surrounds the doped region.

19. (Previously Presented): The bond pad of claim 12 wherein the conductive tap region is a discontinuous region.

20. (Previously Presented): The bond pad of claim 19 wherein the conductive tap region substantially surrounds the doped region in a concentric-like manner.

21. (Previously Presented): The bond pad of claim 12 wherein the conductive region is polysilicon.

22. (Previously Presented): The bond pad of claim 21 wherein the conductive tap region is a doped layer positioned beneath the conductive region.

23. (Presently Amended): A transistor layout for an integrated circuit device having a bond pad, the transistor layout comprising:

a drain region having a first conductivity type doping, wherein the drain region is formed in a semiconductor substrate region having a second conductivity type doping, the drain region being electrically coupled to the bond pad including a metal;

a source region including a second conductivity type doping; and

a conductive tap region spaced proximal to and surrounding the drain region, wherein the conductive tap region is electrically coupled to a supply voltage and electrically and physically coupled to the source region, wherein a section of the conductive tap region is structurally integrated with the source region.

24. (Presently Amended): The transistor layout of claim 23 wherein the supply voltage is a ground voltage and the metal is aluminum.

26. (Previously Presented): The transistor layout of claim 23 wherein the conductive tap region is spaced proximal to and completely surrounds the drain region.

27. (Previously Presented): The transistor layout of claim 23 wherein the conductive tap region is a discontinuous region.

28. (Previously Presented): The transistor layout of claim 23 further including:

a plurality of source regions, each source region of the plurality of source regions being electrically and physically coupled to the conductive tap region;

a plurality of drain regions, each drain region of the plurality of drain regions being electrically coupled to the bond pad; and

wherein the conductive tap region is spaced proximal to and surrounds at least one drain region of the plurality of drain regions.

29. (Previously Presented): The transistor layout of claim 23 wherein the source region includes the first conductivity type doping.

30. (Previously Presented): The transistor layout of claim 23 wherein the conductive tap region is contiguous through a length of the source region.

31. (Previously Presented): The transistor layout of claim 23 further including a conductivity tap region portion spaced proximal to the drain region, wherein the conductive tap region portion is electrically decoupled from the supply voltage and physically decoupled from the conductive tap region.

32. (Previously Presented): The transistor layout of claim 31 wherein the conductive tap region portion is electrically decoupled from the supply voltage and physically decoupled from the conductive tap region using a metal mask option.

33. (Previously Presented): The transistor layout of claim 23 wherein the first conductivity type doping is N type doping and the second conductivity type doping is P type doping.

34. (Previously Presented): The integrated circuit device of claim 9 wherein the tap region portion is physically separate from the first tap region.

35. (Previously Presented): The integrated circuit device of claim 16 wherein the conductive tap region portion is decoupled from the first supply voltage using a metal mask option.

36. (Previously Presented): The bond pad of claim 16 wherein the conductive tap region portion is physically separate from the conductive tap region.

37. (Previously Presented): The bond pad of claim 16 wherein the conductive tap region portion is decoupled from the supply voltage using a metal mask option.

38. (Presently Added): An integrated circuit device, comprising:

a bond pad structure including:

a conductive pad capable to receive a high frequency signal on a line having a first frequency response;

a first doped region of a first conductivity type disposed in a semiconductor substrate of a second conductivity type, wherein the first doped region is underlying and surrounding the conductive pad;

a conductive region of the first conductivity type having a first resistance disposed in the first doped region;

a first tap region positioned from the first doped region to form a second resistance, wherein the first tap region is electrically coupled to a first supply voltage; and,

wherein the first resistance and second resistance are selected to provide a second frequency response of the bond pad structure that substantially matches the first frequency response.

39. (Presently Added): The integrated circuit device of claim 38 wherein the high frequency signal has a frequency higher than approximately 200 Mhz.

40. (Presently Added): The integrated circuit device of claim 38 wherein the high frequency signal has a frequency between approximately 200 Mhz and approximately 1.2 Ghz.

41. (Presently Added): The integrated circuit device of claim 38 wherein the line is included in a controlled impedance bus.

42. (Presently Added): The integrated circuit device of claim 38 wherein an equivalent resistance of the first resistance and second resistance is between approximately 5 ohms and approximately 15 ohms.

43. (Presently Added): The integrated circuit device of claim 38 wherein an equivalent resistance of the first resistance and second resistance is less than approximately 10 ohms.

44. (Presently Added): The integrated circuit device of claim 38 wherein the conductive pad includes a metal.

45. (Presently Added): The integrated circuit device of claim 38 wherein the metal is aluminum.